



LC720DUC

Product Specification

SPECIFICATION FOR APPROVAL

 Preliminary Specification Final Specification

Title	72.0" WUXGA TFT LCD	
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BUYER	General	SUPPLIER	LG.Display Co., Ltd.
MODEL		*MODEL	LC720DUC
		SUFFIX	SCM1

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE DATE
/	
/	
/	
Please return 1 copy for your confirmation with your signature and comments.	

APPROVED BY	SIGNATURE DATE
P.Y. Kim / Team Leader	
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RECORD OF REVISIONS

Revision No.	Revision Date	Page	Description
0.1	DEC, 30, 2009	-	Preliminary Specification(First Draft)
0.2	Feb, 04, 2010	14	3-2-3. Local Dimming Interface revise
		27~28	Mechanical dimmension update
		34	# APPENDIX-I, add Pallet Ass'y
		37~39	# APPENDIX-IV, Local Dimming Interface Design Guide revise
0.3	May, 06, 2010	29	vibration, shock test condition update
		6	Table 2. ELECTRICAL CHARACTERISTICS
		20	3-6. Power Sequence T3 change
		14	Local dimming pin map change
		9~12	Source FFC Pin map change
		37	Local dimming command byte change

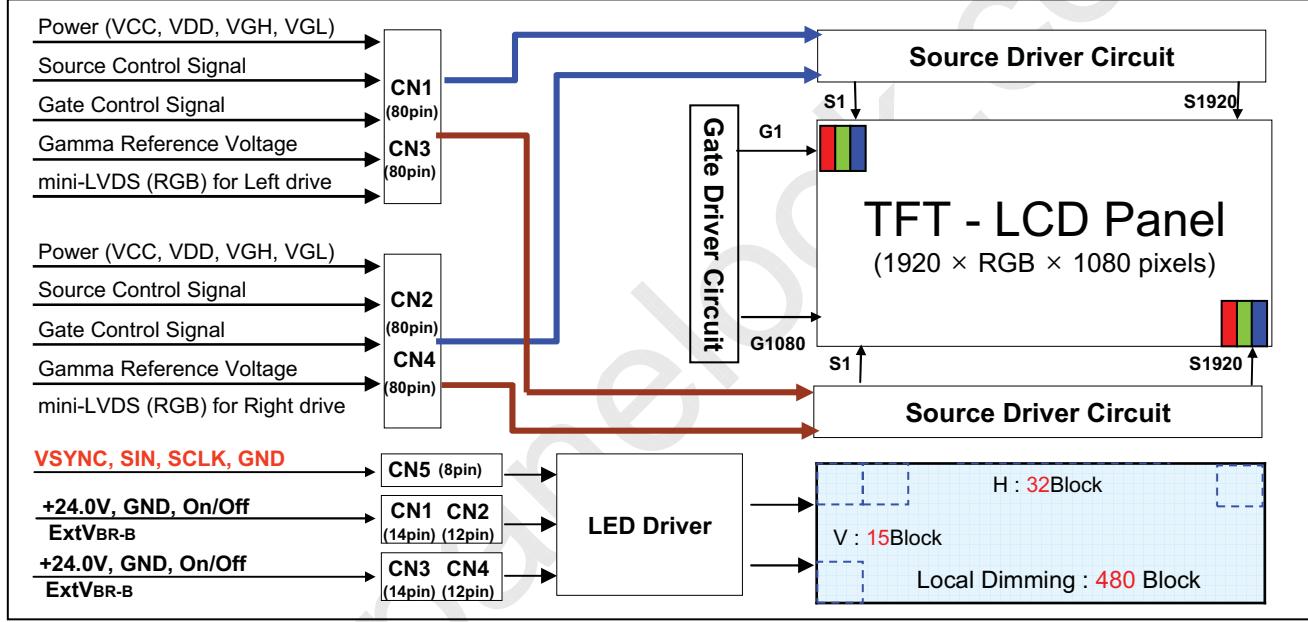
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1. General Description

The LC720DUC is a Color Active Matrix Liquid Crystal Display with an integral Light Emitting Diode (LED) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 72.07 inch diagonally measured active display area with WUXGA resolution (1080 vertical by 1920 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot. Therefore, it can present a palette of more than 16.7M(true) colors.

It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	72.07 inches(1830.616mm) diagonal
Outline Dimension	1666.0(H) x 968.0 (V) x 60.0 mm(D) (Typ.)
Pixel Pitch	0.831 mm x 0.831 mm
Pixel Format	1920 horiz. by 1080 vert. Pixels, RGB stripe arrangement
Color Depth	8-bit, 16.7 M colors (※ 1.06B colors @ 10 bit (D) System Output)
Drive IC Data Interface	Source D-IC : 8-bit mini-LVDS, gamma reference voltage, and control signals
Luminance, White	500 cd/m ² (Center 1point ,Typ.)
Viewing Angle (CR>10)	Viewing angle free (R/L 178 (Min.), U/D 178 (Min.))
Power Consumption	Total 456W(TBD) (Typ.) (Logic=22 W with T-CON , LED Driver =434W(TBD) @EXTVBR-B = 100%)
Weight	37Kg (Typ.)
Display Mode	Transmissive mode, Normally black
Surface Treatment	Hard coating(3H), Anti-glare treatment of the front polarizer (Haze 10%)

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2. Absolute Maximum Ratings

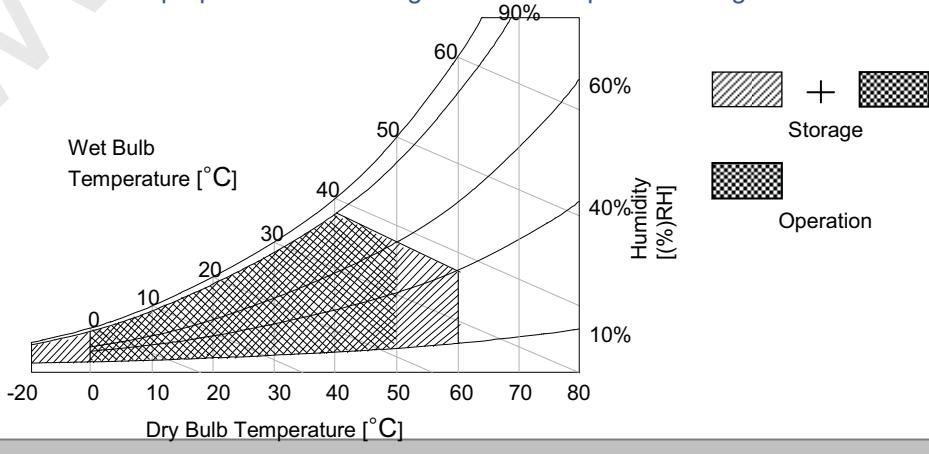
The following items are maximum values which, if exceeded, may cause faulty operation or damage to the LCD module.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value		Unit	Note
		Min	Max		
LED Driver Power Input Voltage	VBL	-0.3	+27.0	VDC	
LED Driver Control Voltage	V _{OFF} / V _{ON}	-0.3	+5.5	VDC	
Brightness	EXTV _{BR-B}	0.0	+5.5	VDC	
Logic Power Voltage	VCC	-0.5	+4.0	Vdc	
Gate High Voltage	VGH	+18.0	+30.0	Vdc	1
Gate Low Voltage	VGL	-8.0	-4.0	Vdc	
Source D-IC Analog Voltage	VDD	-0.3	+18.0	VDC	
Gamma Ref. Voltage (Upper)	VGMH	½VDD-0.5	VDD+0.5	VDC	
Gamma Ref. Voltage (Low)	VGML	-0.3	½ VDD+0.5	Vdc	
Panel Front Temperature	T _{SUR}	-	+68	°C	4
Operating Temperature	T _{OP}	0	+50	°C	
Storage Temperature	T _{ST}	-20	+60	°C	
Operating Ambient Humidity	H _{OP}	10	90	%RH	2,3
Storage Humidity	H _{ST}	10	90	%RH	

Note: 1. Ambient temperature condition ($T_a = 25 \pm 2$ °C)

2. Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be Max 39 °C and no condensation of water.
3. Gravity mura can be guaranteed below 40°C condition.
4. The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 68 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 68 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.



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3. Electrical Specifications**3-1. Electrical Characteristics**

It requires several power inputs. The VCC is the basic power of LCD Driving power sequence, Which is used to logic power voltage of Source D-IC and Gate D-IC.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Logic Power Voltage	VCC	-	3.0	3.3	3.6	VDC	
Logic High Level Input Voltage	VIH		2.7		VCC	VDC	
Logic Low Level Input Voltage	VIL		0		0.6	VDC	
Source D-IC Analog Voltage	VDD	-	Typ.-200mV	16.6	Typ.+200mV	VDC	
Half Source D-IC Analog Voltage	H_VDD	-	GMA10+50mV	8.2	GMA9-50mV	VDC	
Gamma Reference Voltage	V _{GMH}	(GMA1 ~ GMA9)	½*VDD		VDD-0.2		
	V _{GML}	(GMA10 ~ GMA18)	0.2		½*VDD		
Common Voltage	Vcom	-	Typ.-300mV	6.0(TBD)	Typ.+300mV	V	
Mini-LVDS Clock frequency	CLK	3.0V≤VCC ≤3.6V				MHz	
mini-LVDS input Voltage (Center)	V _{IB}	Mini-LVDS Clock and Data	0.7 + (VID/2)		(VCC-1.2) - VID / 2	V	5
mini-LVDS input Voltage Distortion (Center)	ΔV _{IB}				0.8	V	
mini-LVDS differential Voltage range	V _{ID}		150		800	mV	
mini-LVDS differential Voltage range Dip	ΔV _{ID}		25		800	mV	
Gate High Voltage	V _{GH}		Typ.-300mV	26.5	Typ.+300mV	VDC	
Gate Low Voltage	V _{GL}		Typ.-200mV	-5	Typ.+200mV	VDC	
Gate High Modulation Voltage	V _{GHM}			(TBD)		V	
Total Power Current	I _{LCD}	-		TBD		mA	2
Total Power Consumption	P _{LCD}	-		TBD		Watt	2

Note: 1. The specified current and power consumption are under the $V_{LCD}=12V$., $25 \pm 2^{\circ}C$, $f_v=240Hz$ condition whereas mosaic pattern(8 x 6) is displayed and f_v is the frame frequency.

2. The above spec is based on the basic model.
3. All of the typical gate voltage should be controlled within 1% voltage level
4. Ripple voltage level is recommended under 10%
5. In case of mini-LVDS signal spec, refer to Fig 2 for the more detail.
6. Logic Level Input Signal : SOE,POL,GSP,H_CONV,OPT_N

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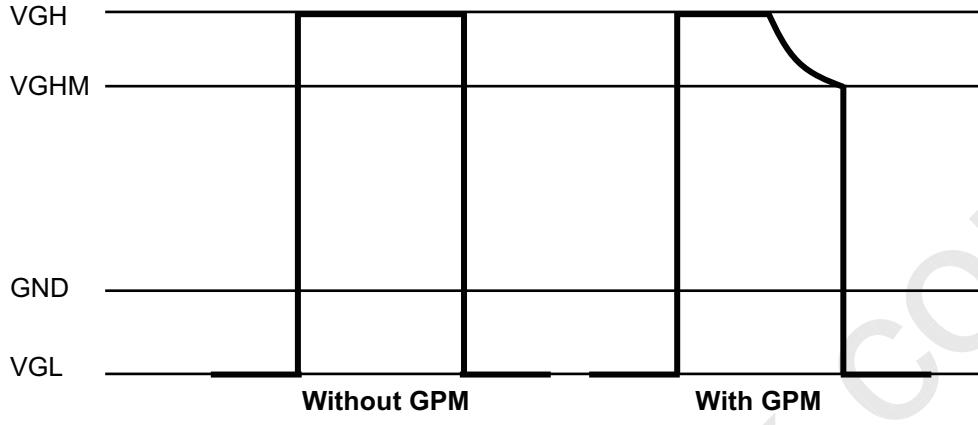
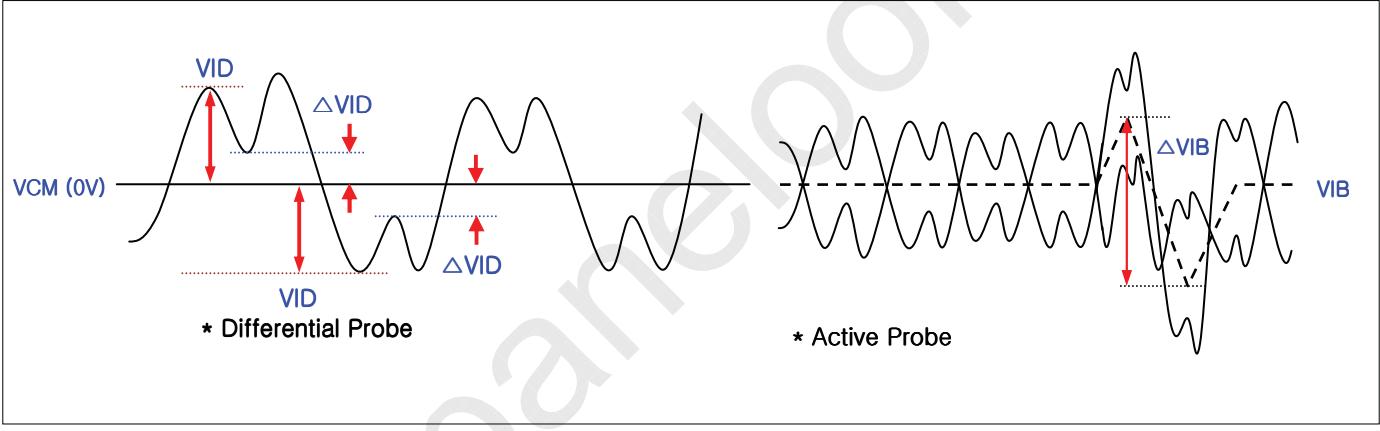


FIG. 1 Gate Output Wave form without GPM and with GPM

FIG. 2 Description of VID, Δ VIB, Δ VID

* Source PCB

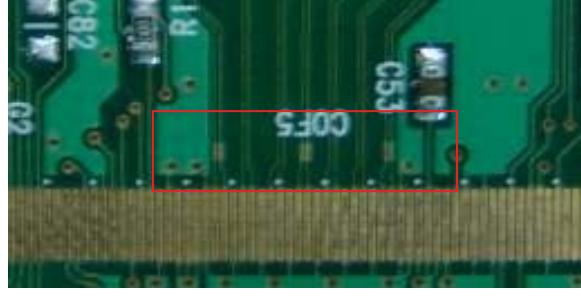


FIG. 3 Measure point

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Table 3. ELECTRICAL CHARACTERISTICS (Continue)

Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
LED Driver :						
Power Supply Input Voltage	VBL	22.8	24.0	25.2	Vdc	1
Power Supply Input Current	IBL_A	-	18.1	19.2 (TBD)	A	Ext VBR-B = 100%
Power Supply Input Current (In-Rush)	Irush	-	-	25.7 (TBD)	A	VBL = 22.8V Ext VBR-B = 100% 4
Power Consumption	PBL	-	434	461 (TBD)	W	Ext VBR-B = 100%
Input Voltage for Control System Signals	On/Off	On	V on	2.5	-	5.0
		Off	V off	-0.3	0.0	0.5
	Brightness Adjust	ExtVBR-B	10	-	100	%
	PWM Frequency for NTSC & PAL	PAL		200		Hz
		NTSC		240		Hz
	Pulse Duty Level (PWM)	High Level	2.5	-	5.0	Vdc
		Low Level	0.0	-	0.5	Vdc
	VSYNC, SIN, SCLK, Reverse (Local Dimming)	High Level	2.7	3.3	3.6	Vdc
		Low Level	-0.3	0.0	0.4	Vdc
LED :						
Life Time		30,000			Hrs	2

Notes :

- Electrical characteristics are determined after the unit has been 'ON' and stable for approximately 60 minutes at $25 \pm 2^\circ\text{C}$. The specified current and power consumption are under the typical supply Input voltage 24V and VBR (ExtVBR-B : 100%), it is total power consumption.
- The life time(MTTF) is determined as the time which luminance of the LED is 50% compared to that of initial value at the typical LED current (ExtVBR-B :100%) on condition of continuous operating in LCM state at $25 \pm 2^\circ\text{C}$.
- LGD recommend that the PWM freq. is synchronized with One time harmonic of Vsync signal of system. Though PWM frequency is over 252Hz(Max), function of LED Driver is not affected.
- The duration of rush current is about 10ms.
- Even though inrush current is over the specified value, there is no problem if I^2T spec of fuse is satisfied.

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3-2. Interface Connections

This LCD module employs two kinds of interface connection, two **80-pin FFC connector** are used for the module electronics and **12-pin,14-pin** connectors are used for the integral backlight system.

3-2-1. LCD Module

-LCD Connector (CN1): TF06L-80S-0.5SH (Manufactured by Hirose) or Equivalent

Table 4-1. MODULE CONNECTOR(CN1) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	VDD	Driver Power Supply Voltage	41	GND	Ground
2	VDD	Driver Power Supply Voltage	42	POL_UP	Polarity Output Signal
3	GND	Ground	43	GSP	Gate Start Pulse
4	VCC	Logic Power Supply Voltage	44	H_CONV	Horizontal 2 Inversion Signal
5	VCC	Logic Power Supply Voltage	45	OPT_N	"H" Normal Display / "L" Rotation Display
6	GND	Ground	46	GND	Ground
7	HVDD	Half Driver Power Supply Voltage	47	LRV5 -	Left Right Mini LVDS Receiver Signal(5-)
8	HVDD	Half Driver Power Supply voltage	48	LRV5 +	Left Right Mini LVDS Receiver Signal(5+)
9	GND	Ground	49	LRV4 -	Left Right Mini LVDS Receiver Signal(4-)
10	VGL	Gate Low Voltage	50	LRV4 +	Left Right Mini LVDS Receiver Signal(4+)
11	GND	Ground	51	LRV3 -	Left Right Mini LVDS Receiver Signal(3-)
12	GOE	Gate Output Enable	52	LRV3 +	Left Right Mini LVDS Receiver Signal(3+)
13	GSC	Gate Shift Clock	53	GND	Ground
14	GND	Ground	54	LRVCLK -	Left Right Mini LVDS Receiver Clock(-)
15	VGH	Gate High Voltage	55	LRVCLK +	Left Right Mini LVDS Receiver Clock(+)
16	GND	Ground	56	GND	Ground
17	GND	Ground	57	LRV2 -	Left Right Mini LVDS Receiver Signal(2-)
18	VCOM_LL	Left Vcom Output	58	LRV2 +	Left Right Mini LVDS Receiver Signal(2+)
19	GND	Ground	59	LRV1 -	Left Right Mini LVDS Receiver Signal(1-)
20	ZOUT	LTD Output	60	LRV1 +	Left Right Mini LVDS Receiver Signal(1+)
21	NC	No connection	61	LRV0 -	Left Right Mini LVDS Receiver Signal(0-)
22	GND	Ground	62	LRV0 +	Left Right Mini LVDS Receiver Signal(0+)
23	GND	Ground	63	GND	Ground
24	GMA18	Gamma Voltage 18	64	LLV5 -	Left Left Mini LVDS Receiver Signal(5-)
25	GMA16	Gamma Voltage 16	65	LLV5 +	Left Left Mini LVDS Receiver Signal(5+)
26	GMA15	Gamma Voltage 15	66	LLV4 -	Left Left Mini LVDS Receiver Signal(4-)
27	GMA14	Gamma Voltage 14	67	LLV4 +	Left Left Mini LVDS Receiver Signal(4+)
28	GMA13	Gamma Voltage 13	68	LLV3 -	Left Left Mini LVDS Receiver Signal(3-)
29	GMA12	Gamma Voltage 12	69	LLV3 +	Left Left Mini LVDS Receiver Signal(3+)
30	GMA10	Gamma Voltage 10	70	GND	Ground
31	GMA9	Gamma Voltage 9	71	LLVCLK -	Left Left Mini LVDS Receiver Clock(-)
32	GMA7	Gamma Voltage 7	72	LLVCLK +	Left Left Mini LVDS Receiver Clock(+)
33	GMA6	Gamma Voltage 6	73	GND	Ground
34	GMA5	Gamma Voltage 5	74	LLV2 -	Left Left Mini LVDS Receiver Signal(2-)
35	GMA4	Gamma Voltage 4	75	LLV2 +	Left Left Mini LVDS Receiver Signal(2+)
36	GMA3	Gamma Voltage 3	76	LLV1 -	Left Left Mini LVDS Receiver Signal(1-)
37	GMA1	Gamma Voltage 1	77	LLV1 +	Left Left Mini LVDS Receiver Signal(1+)
38	GND	Ground	78	LLV0 -	Left Left Mini LVDS Receiver Signal(0-)
39	GND	Ground	79	LLV0 +	Left Left Mini LVDS Receiver Signal(0+)
40	SOE_UL	Source Output Enable	80	GND	Ground

Note : 1. Please refer to application note (**Half VDD & Gamma Voltage setting & Control signal**) for details.

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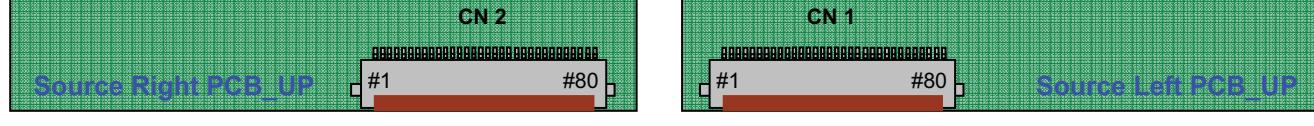
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-LCD Connector (CN2): TF06L-80S-0.5SH (Manufactured by Hirose) or Equivalent

Table 4-2. MODULE CONNECTOR(CN2) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	WP_M	EEPROM Write Protection	41	SOE_UR	Source Output Enable
2	SCL_M	I2C CLOCK	42	GND	Ground
3	SDA_M	I2C DATA	43	POL_UP	Polarity Output Signal
4	GND	Ground	44	GSP	Gate Start Pulse
5	RRV5 -	Right Right Mini LVDS Receiver Signal(5-)	45	GND	Ground
6	RRV5 +	Right Right Mini LVDS Receiver Signal(5+)	46	GMA 18	Gamma Voltage 18
7	RRV4 -	Right Right Mini LVDS Receiver Signal(4-)	47	GMA 16	Gamma Voltage 16
8	RRV4 +	Right Right Mini LVDS Receiver Signal(4+)	48	GMA 15	Gamma Voltage 15
9	RRV3 -	Right Right Mini LVDS Receiver Signal(3-)	49	GMA 14	Gamma Voltage 14
10	RRV3 +	Right Right Mini LVDS Receiver Signal(3+)	50	GMA 13	Gamma Voltage 13
11	GND	Ground	51	GMA 12	Gamma Voltage 12
12	RRVCLK -	Right Right Mini LVDS Receiver Clock(-)	52	GMA 10	Gamma Voltage 10
13	RRVCLK +	Right Right Mini LVDS Receiver Clock(+)	53	GMA 9	Gamma Voltage 9
14	GND	Ground	54	GMA 7	Gamma Voltage 7
15	RRV2 -	Right Right Mini LVDS Receiver Signal(2-)	55	GMA 6	Gamma Voltage 6
16	RRV2 +	Right Right Mini LVDS Receiver Signal(2+)	56	GMA 5	Gamma Voltage 5
17	RRV1 -	Right Right Mini LVDS Receiver Signal(1-)	57	GMA 4	Gamma Voltage 4
18	RRV1 +	Right Right Mini LVDS Receiver Signal(1+)	58	GMA 3	Gamma Voltage 3
19	RRV0 -	Right Right Mini LVDS Receiver Signal(0-)	59	GMA 1	Gamma Voltage 1
20	RRV0 +	Right Right Mini LVDS Receiver Signal(0+)	60	NC	No connection
21	GND	Ground	61	ZOUT	LTD Output
22	RLV5 -	Right Left Mini LVDS Receiver Signal(5-)	62	GND	Ground
23	RLV5 +	Right Left Mini LVDS Receiver Signal(5+)	63	VCOM_R	Right Vcom Output
24	RLV4 -	Right Left Mini LVDS Receiver Signal(4-)	64	GND	Ground
25	RLV4 +	Right Left Mini LVDS Receiver Signal(4+)	65	VGH	Gate High Voltage
26	RLV3 -	Right Left Mini LVDS Receiver Signal(3-)	66	GND	Ground
27	RLV3 +	Right Left Mini LVDS Receiver Signal(3+)	67	GSC	Gate Shift Clock
28	GND	Ground	68	GOE	Gate Output Enable
29	RLVCLK -	Right Left Mini LVDS Receiver Clock(-)	69	GND	Ground
30	RLVCLK +	Right Left Mini LVDS Receiver Clock(+)	70	VGL	Gate Low Voltage
31	GND	Ground	71	OPT_P	"L" Normal Display / "H" Rotation Display
32	RLV2 -	Right Left Mini LVDS Receiver Signal(2-)	72	GND	Ground
33	RLV2 +	Right Left Mini LVDS Receiver Signal(2+)	73	HVDD	Half Driver Power Supply Voltage
34	RLV1 -	Right Left Mini LVDS Receiver Signal(1-)	74	HVDD	Half Driver Power Supply voltage
35	RLV1 +	Right Left Mini LVDS Receiver Signal(1+)	75	GND	Ground
36	RLV0 -	Right Left Mini LVDS Receiver Signal(0-)	76	VCC	Logic Power Supply Voltage
37	RLV0 +	Right Left Mini LVDS Receiver Signal(0+)	77	VCC	Logic Power Supply Voltage
38	GND	Ground	78	GND	Ground
39	OPT_N	"H" Normal Display / "L" Rotation Display	79	VDD	Driver Power Supply Voltage
40	H_CONV	Horizontal 2 Inversion Signal	80	VDD	Driver Power Supply Voltage

Note : 1. Please refer to application note (**Half VDD & Gamma Voltage setting & Control signal**) for details.



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-LCD Connector (CN3): TF06L-80S-0.5SH (Manufactured by Hirose) or Equivalent

Table 4-3. MODULE CONNECTOR(CN3) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	WP_S	EEPROM Write Protection	41	SOE_DL	Source Output Enable
2	SCL_S	I2C CLOCK	42	GND	Ground
3	SDA_S	I2C DATA	43	POL_DOWN	Polarity Output Signal
4	GND	Ground	44	GND	Ground
5	RRV5 -	Left Right Mini LVDS Receiver Signal(5-)	45	GND	Ground
6	RRV5 +	Left Right Mini LVDS Receiver Signal(5+)	46	GMA 18	Gamma Voltage 18
7	RRV4 -	Left Right Mini LVDS Receiver Signal(4-)	47	GMA 16	Gamma Voltage 16
8	RRV4 +	Left Right Mini LVDS Receiver Signal(4+)	48	GMA 15	Gamma Voltage 15
9	RRV3 -	Left Right Mini LVDS Receiver Signal(3-)	49	GMA 14	Gamma Voltage 14
10	RRV3 +	Left Right Mini LVDS Receiver Signal(3+)	50	GMA 13	Gamma Voltage 13
11	GND	Ground	51	GMA 12	Gamma Voltage 12
12	RRVCLK -	Left Right Mini LVDS Receiver Clock(-)	52	GMA 10	Gamma Voltage 10
13	RRVCLK +	Left Right Mini LVDS Receiver Clock(+)	53	GMA 9	Gamma Voltage 9
14	GND	Ground	54	GMA 7	Gamma Voltage 7
15	RRV2 -	Left Right Mini LVDS Receiver Signal(2-)	55	GMA 6	Gamma Voltage 6
16	RRV2 +	Left Right Mini LVDS Receiver Signal(2+)	56	GMA 5	Gamma Voltage 5
17	RRV1 -	Left Right Mini LVDS Receiver Signal(1-)	57	GMA 4	Gamma Voltage 4
18	RRV1 +	Left Right Mini LVDS Receiver Signal(1+)	58	GMA 3	Gamma Voltage 3
19	RRV0 -	Left Right Mini LVDS Receiver Signal(0-)	59	GMA 1	Gamma Voltage 1
20	RRV0 +	Left Right Mini LVDS Receiver Signal(0+)	60	ZOUT_DOWN	LTD Output
21	GND	Ground	61	NC	No connection
22	RLV5 -	Left Left Mini LVDS Receiver Signal(5-)	62	GND	Ground
23	RLV5 +	Left Left Mini LVDS Receiver Signal(5+)	63	VCOM_R	Right Vcom Output
24	RLV4 -	Left Left Mini LVDS Receiver Signal(4-)	64	GND	Ground
25	RLV4 +	Left Left Mini LVDS Receiver Signal(4+)	65	VGH	Gate High Voltage
26	RLV3 -	Left Left Mini LVDS Receiver Signal(3-)	66	GND	Ground
27	RLV3 +	Left Left Mini LVDS Receiver Signal(3+)	67	GSC	Gate Shift Clock
28	GND	Ground	68	GOE	Gate Output Enable
29	RLVCLK -	Left Left Mini LVDS Receiver Clock(-)	69	GND	Ground
30	RLVCLK +	Left Left Mini LVDS Receiver Clock(+)	70	VGL	Gate Low Voltage
31	GND	Ground	71	OPT_N	"H" Normal Display / "L" Rotation Display
32	RLV2 -	Left Left Mini LVDS Receiver Signal(2-)	72	GND	Ground
33	RLV2 +	Left Left Mini LVDS Receiver Signal(2+)	73	HVDD	Half Driver Power Supply Voltage
34	RLV1 -	Left Left Mini LVDS Receiver Signal(1-)	74	HVDD	Half Driver Power Supply voltage
35	RLV1 +	Left Left Mini LVDS Receiver Signal(1+)	75	GND	Ground
36	RLV0 -	Left Left Mini LVDS Receiver Signal(0-)	76	VCC	Logic Power Supply Voltage
37	RLV0 +	Left Left Mini LVDS Receiver Signal(0+)	77	VCC	Logic Power Supply Voltage
38	GND	Ground	78	GND	Ground
39	OPT_P	"L" Normal Display / "H" Rotation Display	79	VDD	Driver Power Supply Voltage
40	H_CONV	Horizontal 2 Inversion Signal	80	VDD	Driver Power Supply Voltage

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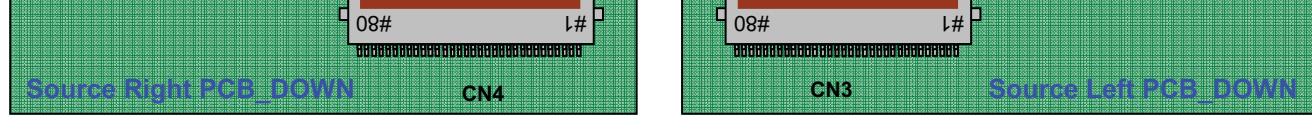
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-LCD Connector (CN2): TF06L-80S-0.5SH (Manufactured by Hirose) or Equivalent

Table 4-4. MODULE CONNECTOR(CN4) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	VDD	Driver Power Supply Voltage	41	GND	Ground
2	VDD	Driver Power Supply Voltage	42	POL_DOWN	Polarity Output Signal
3	GND	Ground	43	NC	No connection
4	VCC	Logic Power Supply Voltage	44	H_CONV	Horizontal 2 Inversion Signal
5	VCC	Logic Power Supply Voltage	45	OPT_P	"L" Normal Display / "H" Rotation Display
6	GND	Ground	46	GND	Ground
7	HVDD	Half Driver Power Supply Voltage	47	LRV5 -	Right Right Mini LVDS Receiver Signal(5-)
8	HVDD	Half Driver Power Supply voltage	48	LRV5 +	Right Right Mini LVDS Receiver Signal(5+)
9	GND	Ground	49	LRV4 -	Right Right Mini LVDS Receiver Signal(4-)
10	VGL	Gate Low Voltage	50	LRV4 +	Right Right Mini LVDS Receiver Signal(4+)
11	GND	Ground	51	LRV3 -	Right Right Mini LVDS Receiver Signal(3-)
12	GOE	Gate Output Enable	52	LRV3 +	Right Right Mini LVDS Receiver Signal(3+)
13	GSC	Gate Shift Clock	53	GND	Ground
14	GND	Ground	54	LRVCLK -	Right Right Mini LVDS Receiver Clock(-)
15	VGH	Gate High Voltage	55	LRVCLK +	Right Right Mini LVDS Receiver Clock(+)
16	GND	Ground	56	GND	Ground
17	GND	Ground	57	LRV2 -	Right Right Mini LVDS Receiver Signal(2-)
18	VCOM_L	Left Vcom Output	58	LRV2 +	Right Right Mini LVDS Receiver Signal(2+)
19	GND	Ground	59	LRV1 -	Right Right Mini LVDS Receiver Signal(1-)
20	NC	No connection	60	LRV1 +	Right Right Mini LVDS Receiver Signal(1+)
21	ZOUT_DOWN	LTD Output	61	LRV0 -	Right Right Mini LVDS Receiver Signal(0-)
22	GND	Ground	62	LRV0 +	Right Right Mini LVDS Receiver Signal(0+)
23	GND	Ground	63	GND	Ground
24	GMA18	Gamma Voltage 18	64	LLV5 -	Right Left Mini LVDS Receiver Signal(5-)
25	GMA16	Gamma Voltage 16	65	LLV5 +	Right Left Mini LVDS Receiver Signal(5+)
26	GMA15	Gamma Voltage 15	66	LLV4 -	Right Left Mini LVDS Receiver Signal(4-)
27	GMA14	Gamma Voltage 14	67	LLV4 +	Right Left Mini LVDS Receiver Signal(4+)
28	GMA13	Gamma Voltage 13	68	LLV3 -	Right Left Mini LVDS Receiver Signal(3-)
29	GMA12	Gamma Voltage 12	69	LLV3 +	Right Left Mini LVDS Receiver Signal(3+)
30	GMA10	Gamma Voltage 10	70	GND	Ground
31	GMA9	Gamma Voltage 9	71	LLVCLK -	Right Left Mini LVDS Receiver Clock(-)
32	GMA7	Gamma Voltage 7	72	LLVCLK +	Right Left Mini LVDS Receiver Clock(+)
33	GMA6	Gamma Voltage 6	73	GND	Ground
34	GMA5	Gamma Voltage 5	74	LLV2 -	Right Left Mini LVDS Receiver Signal(2-)
35	GMA4	Gamma Voltage 4	75	LLV2 +	Right Left Mini LVDS Receiver Signal(2+)
36	GMA3	Gamma Voltage 3	76	LLV1 -	Right Left Mini LVDS Receiver Signal(1-)
37	GMA1	Gamma Voltage 1	77	LLV1 +	Right Left Mini LVDS Receiver Signal(1+)
38	GND	Ground	78	LLV0 -	Right Left Mini LVDS Receiver Signal(0-)
39	GND	Ground	79	LLV0 +	Right Left Mini LVDS Receiver Signal(0+)
40	SOE_DR	Source Output Enable	80	GND	Ground

Note : 1. Please refer to application note (**Half VDD & Gamma Voltage setting & Control signal**) for details.



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Product Specification

3-2-2. Backlight Module**Board A(CN1101), Board B(CN2101)**

- LED Driver Connector : 20022WR-14B1(Yeonho)
or Equivalent
- Mating Connector : 20022HS-14 or Equivalent

Board A(CN1106), Board B(CN2106)

- LED Driver Connector : 20022WR-12B1(Yeonho)
or Equivalent
- Mating Connector : 20022HS-12 or Equivalent

Table 5. LED DRIVER CONNECTOR PIN CONFIGURATION

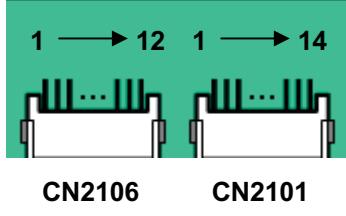
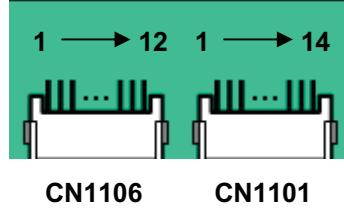
Pin No	Symbol	Description	Board A (CN1101) Board B (CN2101)	Board A (CN1106) Board B (CN2106)	Note
1	VBL	Power Supply +24.0V	VBL	VBL	
2	VBL	Power Supply +24.0V	VBL	VBL	
3	VBL	Power Supply +24.0V	VBL	VBL	
4	VBL	Power Supply +24.0V	VBL	VBL	
5	VBL	Power Supply +24.0V	VBL	VBL	
6	GND	Backlight Ground	GND	GND	
7	GND	Backlight Ground	GND	GND	
8	GND	Backlight Ground	GND	GND	
9	GND	Backlight Ground	GND	GND	
10	GND	Backlight Ground	GND	GND	
11	NC	No connection	OPEN or GND	Don't Care	
12	VON/OFF	Backlight ON/OFF control	VON/OFF	Don't Care	
13	EXTVBR-B	External PWM	EXTVBR-B		2
14	GND	Backlight Ground	GND		3

Notes : 1. GND should be connected to the LCD module's metal frame.

2. High : on duty / Low : off duty, Pin#13 can be opened. (if Pin #13 is open , EXTVBR-B is 100%)

3. #14 of Input CNT Must be Connected to **Backlight Ground**.

4. Each impedance of pin #12 and 13 is over TBD [KΩ] and over TBD [KΩ].

◆ Rear view of LCM**Board B****Board A**

LC720DUC

Product Specification

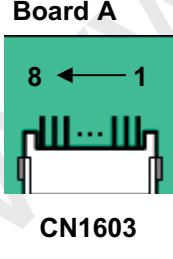
3-2-3. Local Dimming Interface**Board A(CN1603)**

- LED Driver Connector : 12507WR-08L(Yeonho) or Equivalent
- Mating Connector : 12507HS-08L(Yeonho) or Equivalent

Table 5-2. LOCAL DIMMING INTERFACE CONNECTOR PIN CONFIGURATION

Pin No	Symbol	Description	Note
1	VSYNC	Vertical Sync signal	
2	GND	Backlight Ground	1
3	SIN	1'st SPI Data	
4	SCLK	1'st SPI Clock	
5	GND	Backlight Ground	1
6	SIN	2'nd SPI Data	
7	SCLK	2'nd SPI Clock	
8	GND	Backlight Ground	1

Notes : 1. GND should be connected to the LCD module's metal frame.

◆ Rear view of LCM

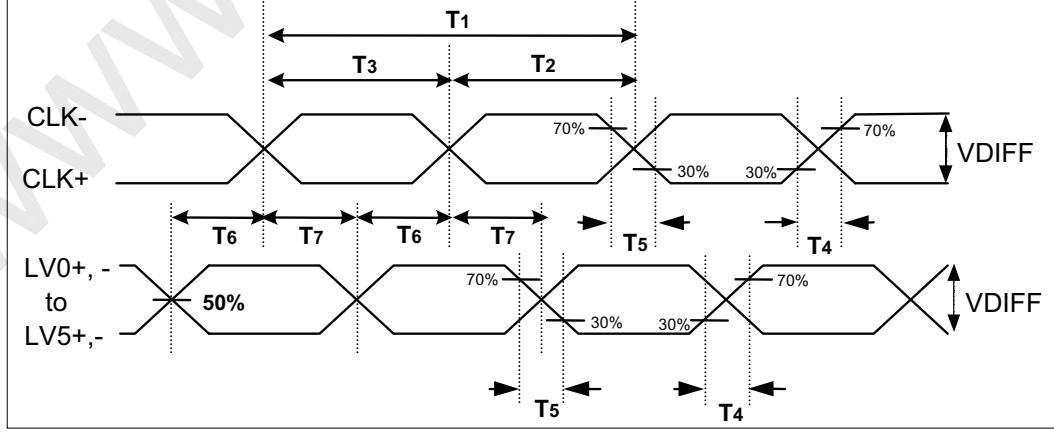
Product Specification

3-3. Signal Timing Specifications**Table 6. Timing Requirements**

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Mini Clock pulse period	T1		3.2	3.4		ns	1
Mini Clock pulse low period	T2		1.6	-	-	ns	
Mini Clock pulse high period	T3		1.6	-	-	ns	
Mini Data setup time	T6		0.6	-	-	ns	
Mini Data hold time	T7		0.6	-	-	ns	
Reset low to SOE rising time	T8		0	-	-	ns	
SOE to Reset input time	T9		200	-	-	ns	
Receiver off to SOE timing	T10		10	-	-	CLK cycle	
POL signal to SOE setup time	T11		-5	-	-	ns	
POL signal to SOE hold time	T12		6	-	-	ns	
Reset High Period	T13		3			CLK cycle	
SOE signal GSP setup time	T14		100			ns	
SOE							
SOE							

Note :

TBD

**FIG 4. Source D-IC Input Data Latch Timing Waveform**

Product Specification

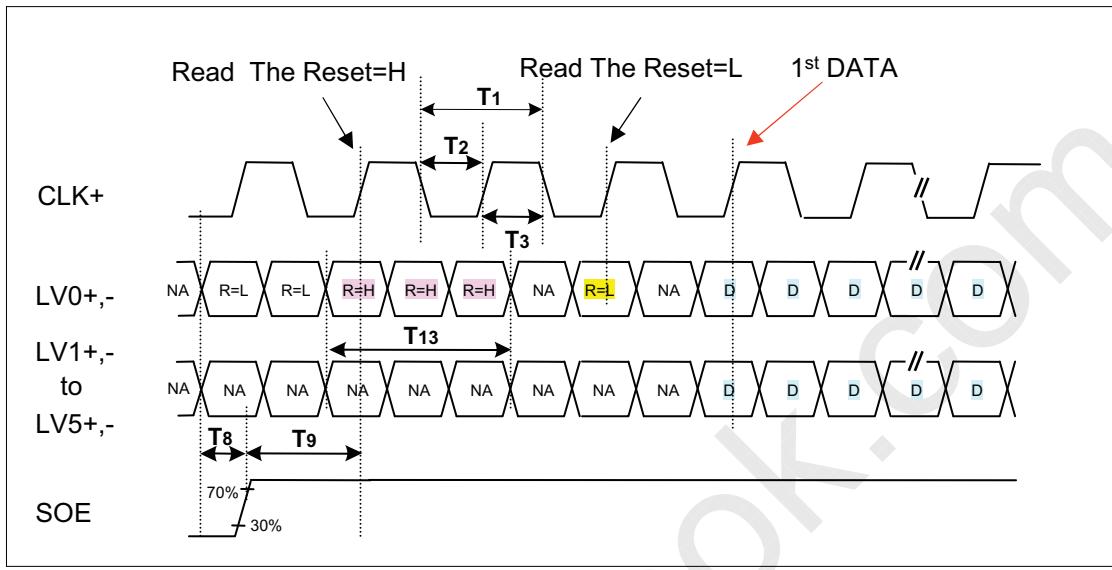
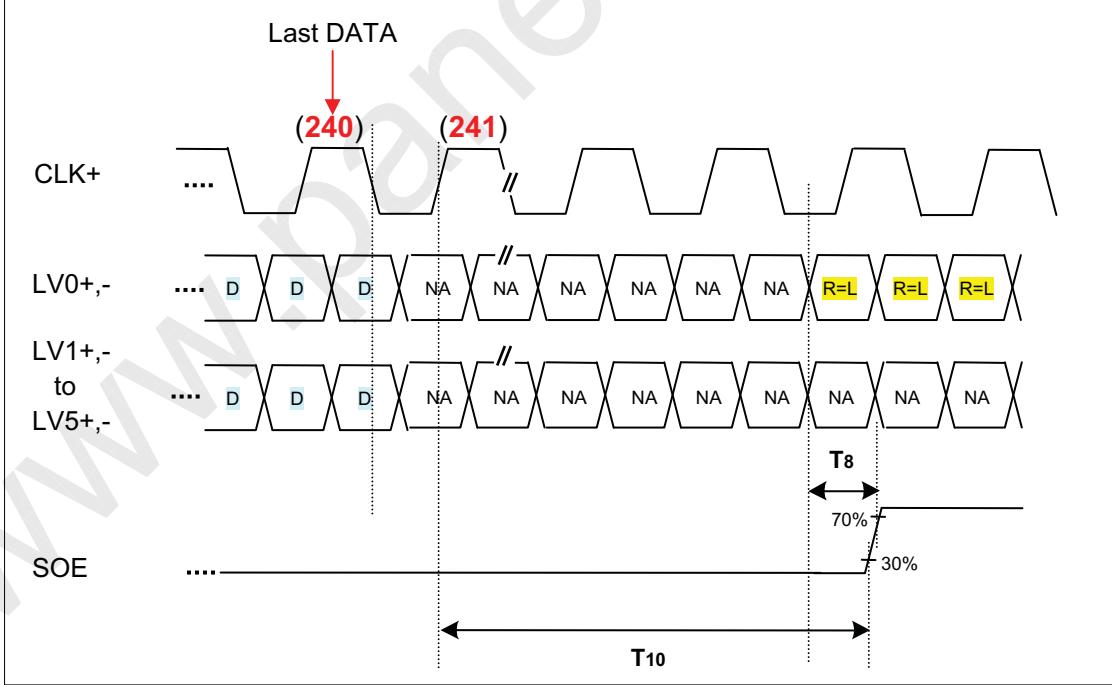
FIG 5-1. Input Data Timing for 1st Source D-IC Chip

FIG 5-2. Last Data Latch to SOE Timing

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Product Specification

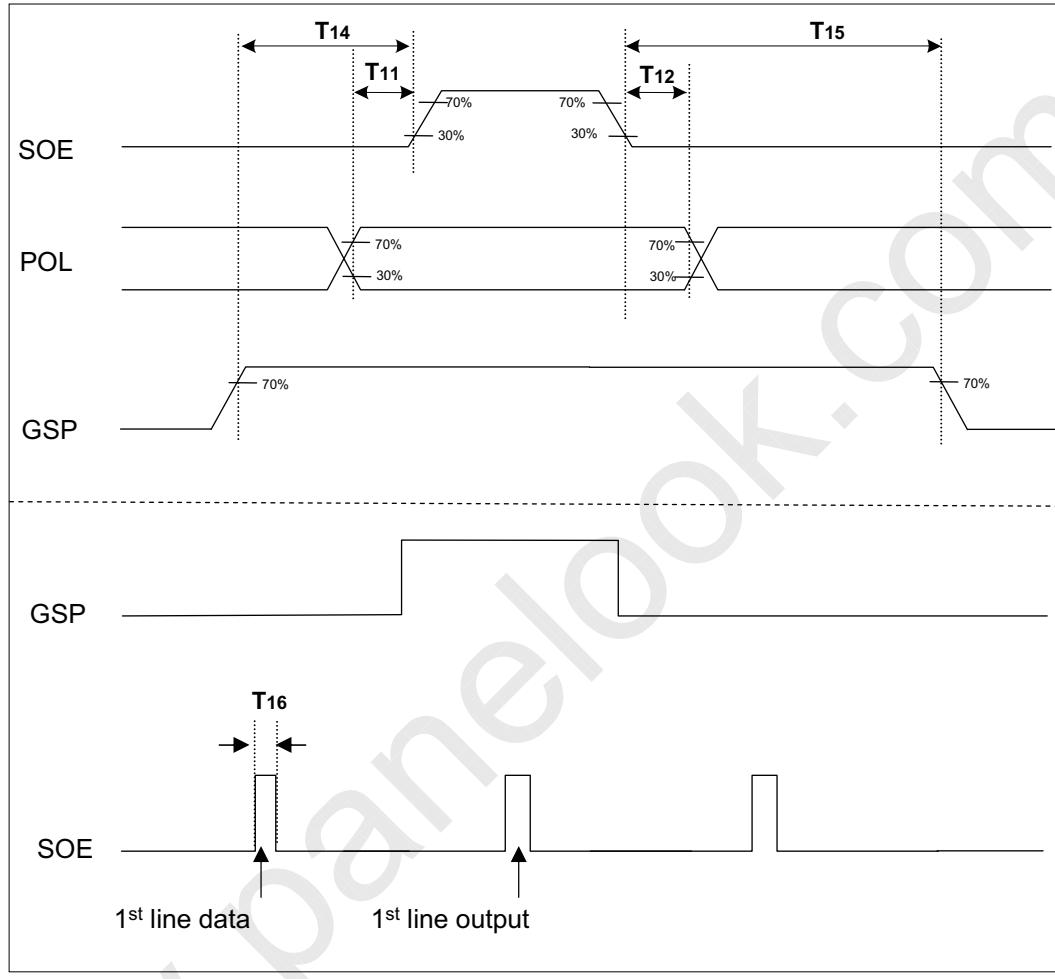


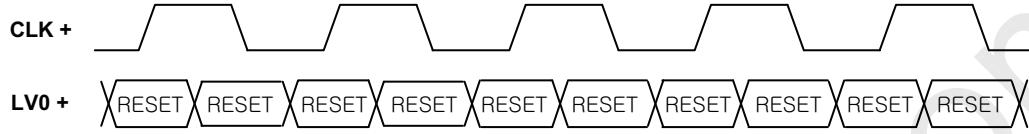
FIG 6. POL, GSP and SOE Timing Waveform

Product Specification

3-4. Data Mapping and Timing

Display data and control signal (RESET) are input to **LV0** to **LV5**.

3-4-1. Control signal input mode



3-4-2. Display data input mode

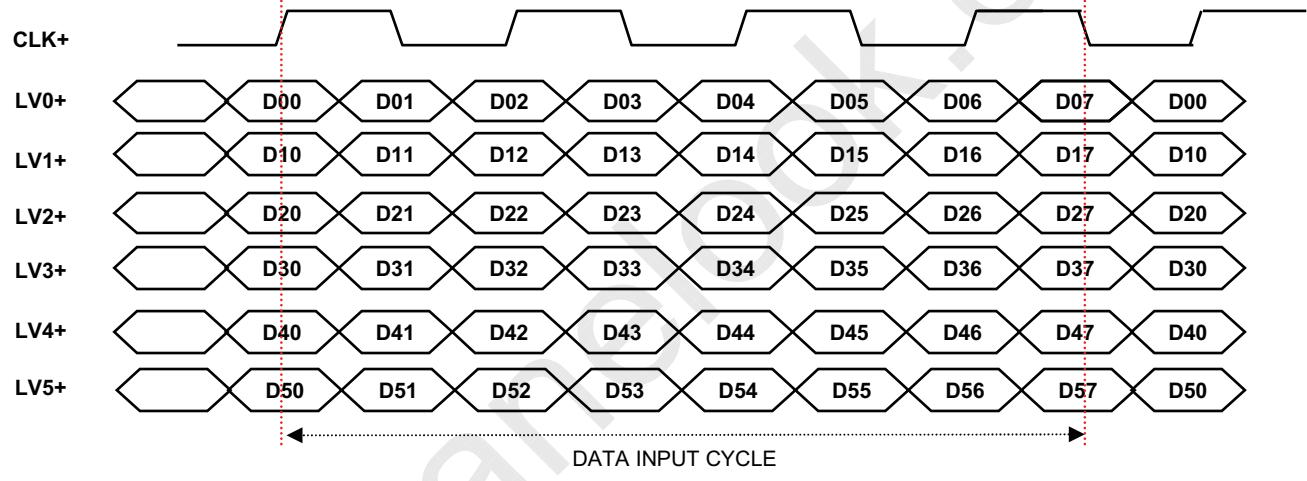


Fig. 7 Mini-LVDS Data

Note : 1. For data mapping, please refer to panel pixel structure Fig.8

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Product Specification

3-5. Panel Pixel Structure

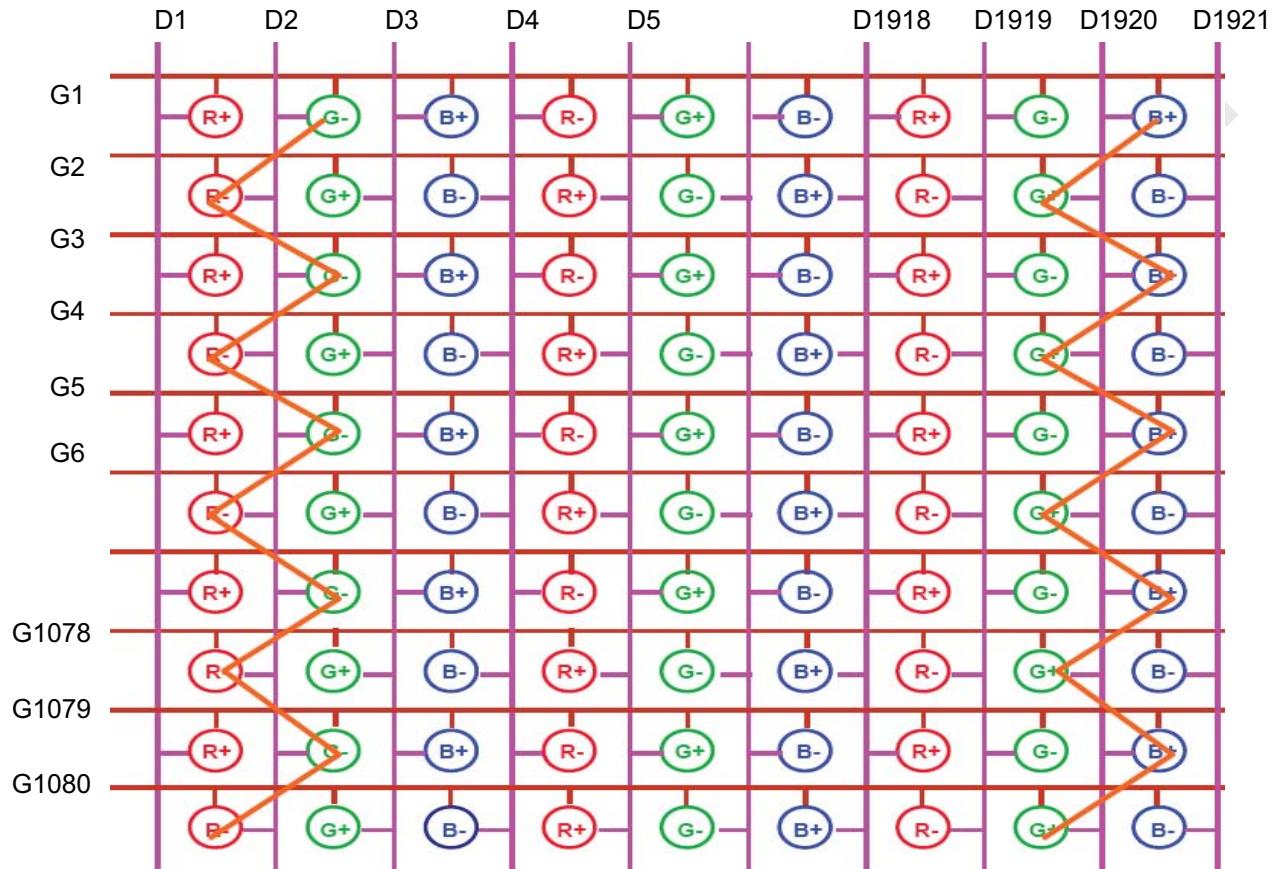
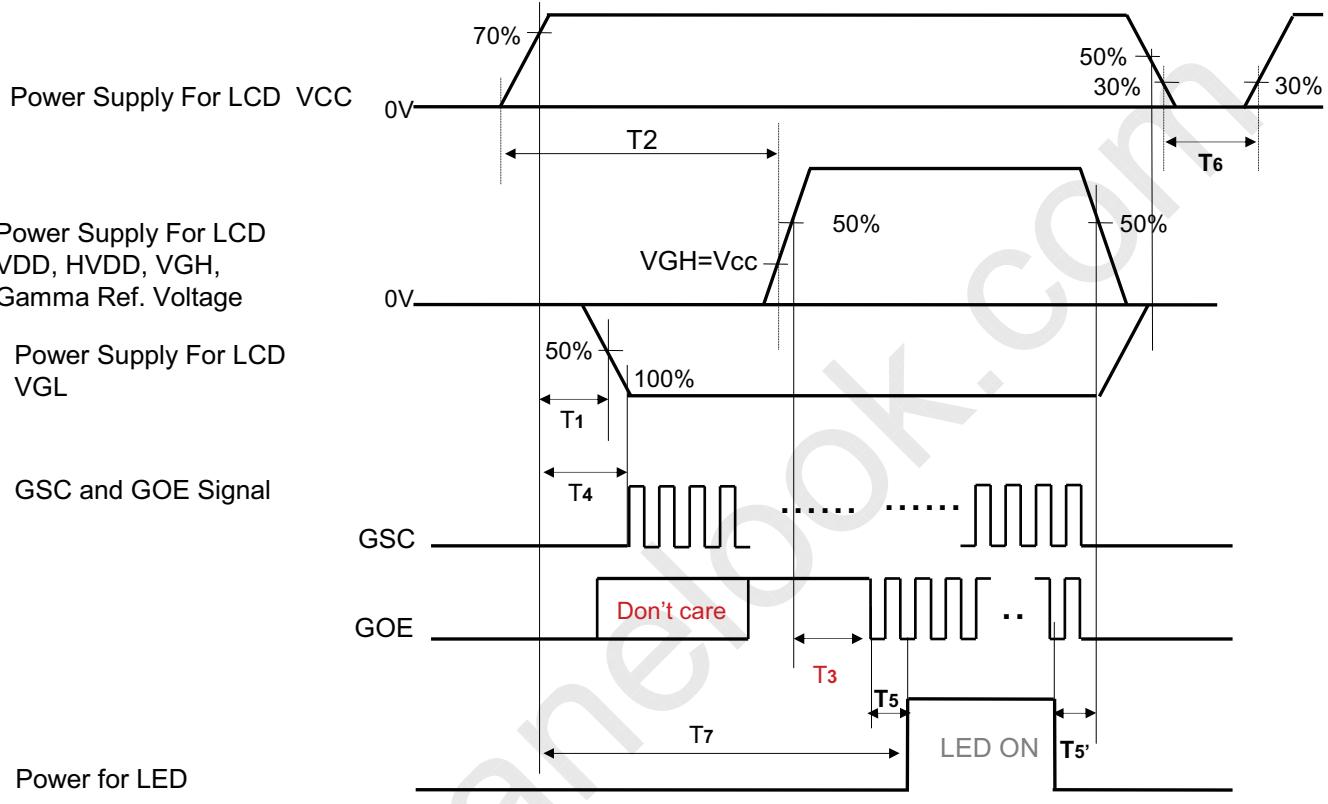


FIG. 8 Panel Pixel Structure

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Product Specification

3-6. Power Sequence**3-6-1. LCD Driving circuit****Table 7. POWER SEQUENCE**

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T_1	0.5		-	ms	
T_2	0.01		-	ms	
T_3	10		-	ms	
T_4	0		T_2	ms	
T_5 / T_5'	20		-	ms	
T_6	2		-	sec	
T_7	0.5		-	s	

Note :

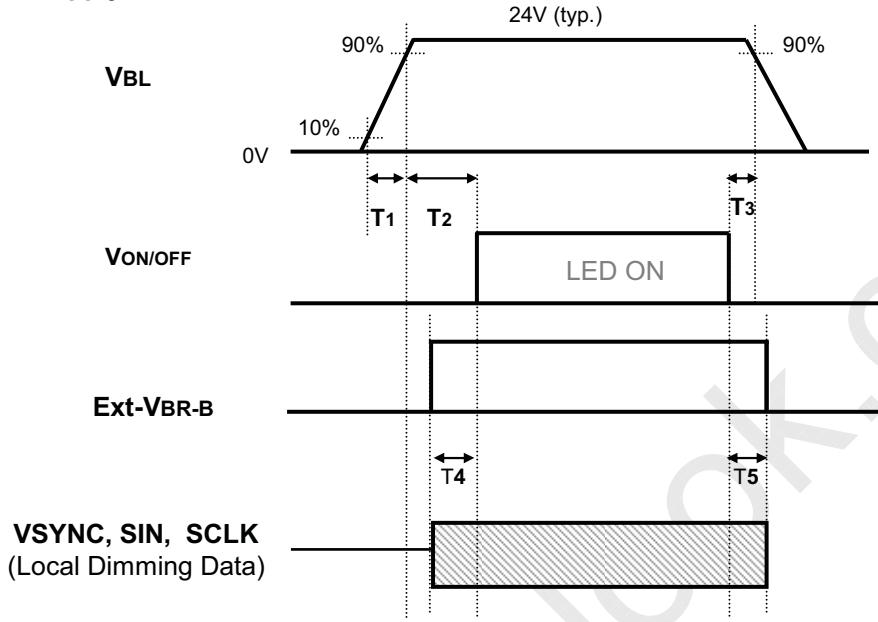
1. Power sequence for Source D-IC must be kept. ※ Please refer to Appendix IV for more details
2. The Gate D-IC power on sequence must be VCC, VGL, logic input & VGH.
3. The 1st start of GSC is located between VGL and VGH.
4. GOE rising is before GSC.
5. Power off sequence order is reverse of power on sequence.

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Product Specification

3-6-2. Sequence for LED Driver

Power Supply For LED Driver



3-6-3. Dip condition for LED Driver

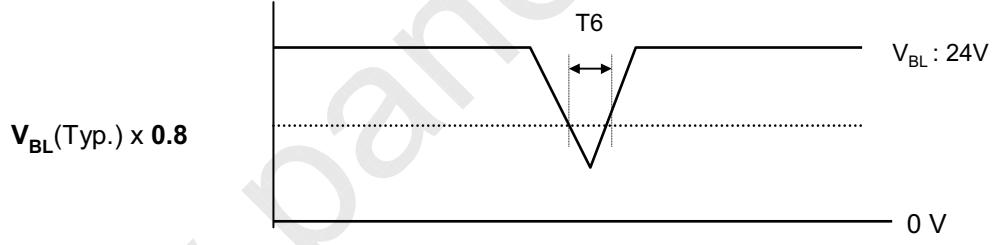


Table 9. Power Sequence for LED Driver

Parameter	Values			Units	Remarks
	Min	Typ	Max		
T1	20	-	-	ms	1
T2	500	-	-	ms	
T3	10	-	-	ms	
T4	0	-	-	ms	
T5	0	-	-	ms	
T6	-	-	10	ms	$V_{BL}(\text{Typ.}) \times 0.8$

Notes : 1. T1 describes rising time of 0V to 24V and this parameter does not apply at restarting time.
Even though T1 is over the specified value, there is no problem if I²T spec of fuse is satisfied.

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Product Specification

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at $25 \pm 2^\circ\text{C}$. The values are specified at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0° .

It is presented additional information concerning the measurement equipment and method in FIG. 1.

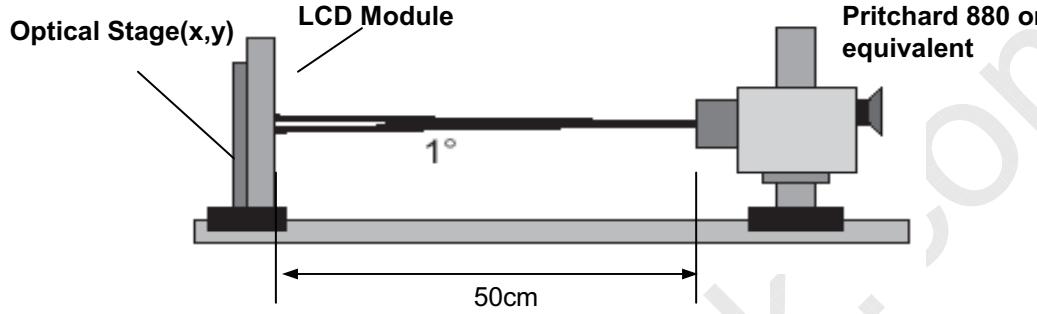


FIG. 1 Optical Characteristic Measurement Equipment and Method

$T_a = 25 \pm 2^\circ\text{C}$, $V_{LCD} = 12.0\text{V}$, $f_v = 240\text{Hz}$, $Dclk = 74.25\text{MHz}$,
 $EXTV_{BR-B} = 100\%$

Table 10. OPTICAL CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Contrast Ratio	CR	TBD	1200	TBD		1
Surface Luminance, white	L_{WH}	400	500	-	cd/m ²	2
Luminance Variation	δ_{WHITE}	5P	-	-	1.3	3
Response Time	Rising	Tr	-	TBD	TBD	ms
	Falling	Tf	-	TBD	TBD	
Color Coordinates [CIE1931]	RED	Rx		TBD		
		Ry		TBD		
	GREEN	Gx		TBD		
		Gy	Typ	TBD	Typ +0.03	
	BLUE	Bx	-0.03	TBD		
		By		TBD		
	WHITE	Wx		0.279		
		Wy		0.292		
Color Temperature				10,000		K
Color Gamut				72		%
Viewing Angle (CR>10)						
	x axis, right($\phi=0^\circ$)	θ_r	89	-	-	degree
	x axis, left ($\phi=180^\circ$)	θ_l	89	-	-	
	y axis, up ($\phi=90^\circ$)	θ_u	89	-	-	
	y axis, down ($\phi=270^\circ$)	θ_d	89	-	-	
Gray Scale			-	-	-	6

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Product Specification

Note : 1. Contrast Ratio(CR) is defined mathematically as :

$$CR = \frac{\text{Surface Luminance at all white pixels}}{\text{Surface Luminance at all black pixels}}$$

It is measured at center 1-point.

2. Surface luminance is determined after the unit has been 'ON' and 1Hour after lighting the backlight in a dark environment at $25 \pm 2^\circ\text{C}$. Surface luminance is the luminance value at center 1-point across the LCD surface 50cm from the surface with all pixels displaying white.
For more information see the FIG. 10.
3. The variation in surface luminance , δ WHITE is defined as :
 δ WHITE(5P) = Maximum($L_{on1}, L_{on2}, L_{on3}, L_{on4}, L_{on5}$) / Minimum($L_{on1}, L_{on2}, L_{on3}, L_{on4}, L_{on5}$)
Where L_{on1} to L_{on5} are the luminance with all pixels displaying white at 5 locations .
For more information, see the FIG. 10.
4. Response time is the time required for the display to transit from G(255) to G(0) (Rise Time, Tr_R) and from G(0) to G(255) (Decay Time, Tr_D).
5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 12.
6. Gray scale specification
Gamma Value is approximately 2.2. For more information, see the Table 10.

Table 10. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ)
L0	0.08
L15	0.28
L31	1.05
L47	2.50
L63	4.69
L79	7.67
L95	11.47
L111	16.11
L127	21.64
L143	28.07
L159	35.43
L175	43.73
L191	52.99
L207	63.23
L223	74.47
L239	86.72
L255	100

	Gray Level	Gamma Ref.
Positive Voltage	L0	Gamma9
	L31	Gamma7
	L63	Gamma6
	L127	Gamma5
	L191	Gamma4
	L223	Gamma3
	L255	Gamma1
	L255	Gamma18
Negative Voltage	L223	Gamma16
	L191	Gamma15
	L127	Gamma14
	L63	Gamma13
	L31	Gamma12
	L0	Gamma10

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Product Specification

Measuring point for surface luminance & luminance variation

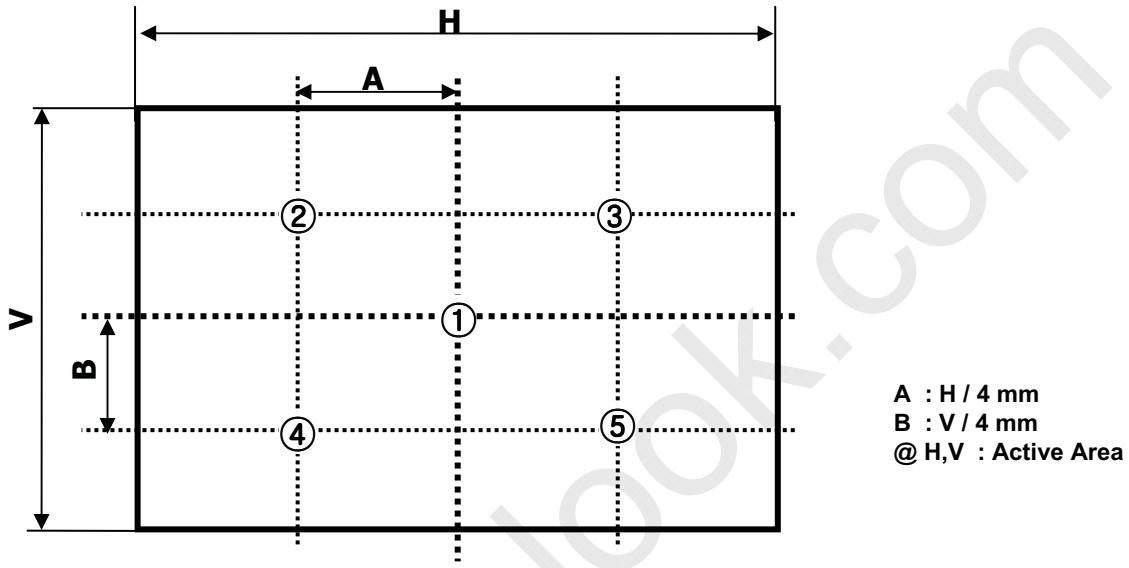


FIG. 10 5 Points for Luminance Measure

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".

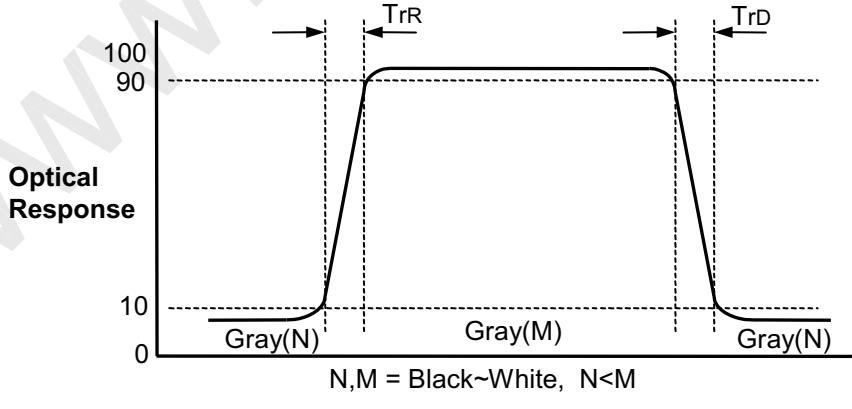


FIG. 11 Response Time

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Product Specification

Dimension of viewing angle range

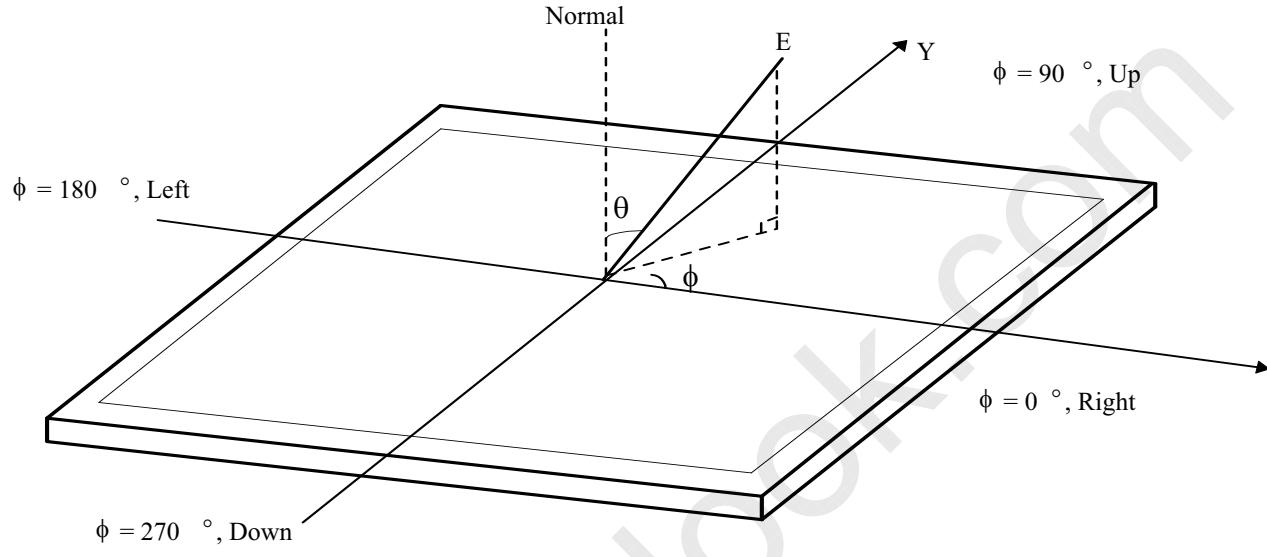


FIG.12 Viewing Angle

LC720DUC

Product Specification

5. Mechanical Characteristics

Table 11 provides general mechanical characteristics.

Table 11. MECHANICAL CHARACTERISTICS

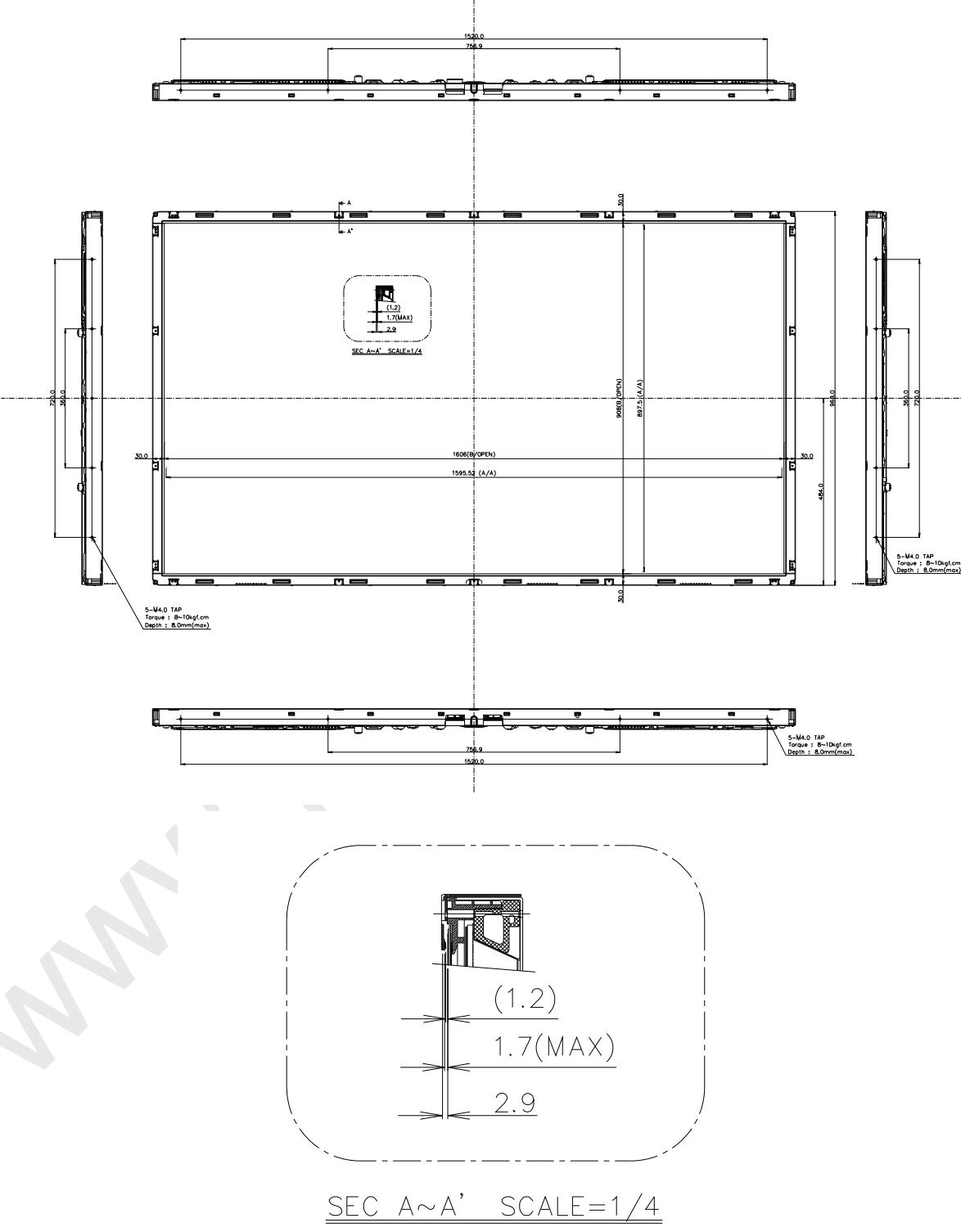
Item	Value	
Outline Dimension	Horizontal	1666.0 mm
	Vertical	968.0 mm
	Depth	60.0 mm
Bezel Area	Horizontal	1606.0mm
	Vertical	908.0mm
Active Display Area	Horizontal	1595.52 mm
	Vertical	897.48 mm
Weight	37kg	

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.

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Product Specification

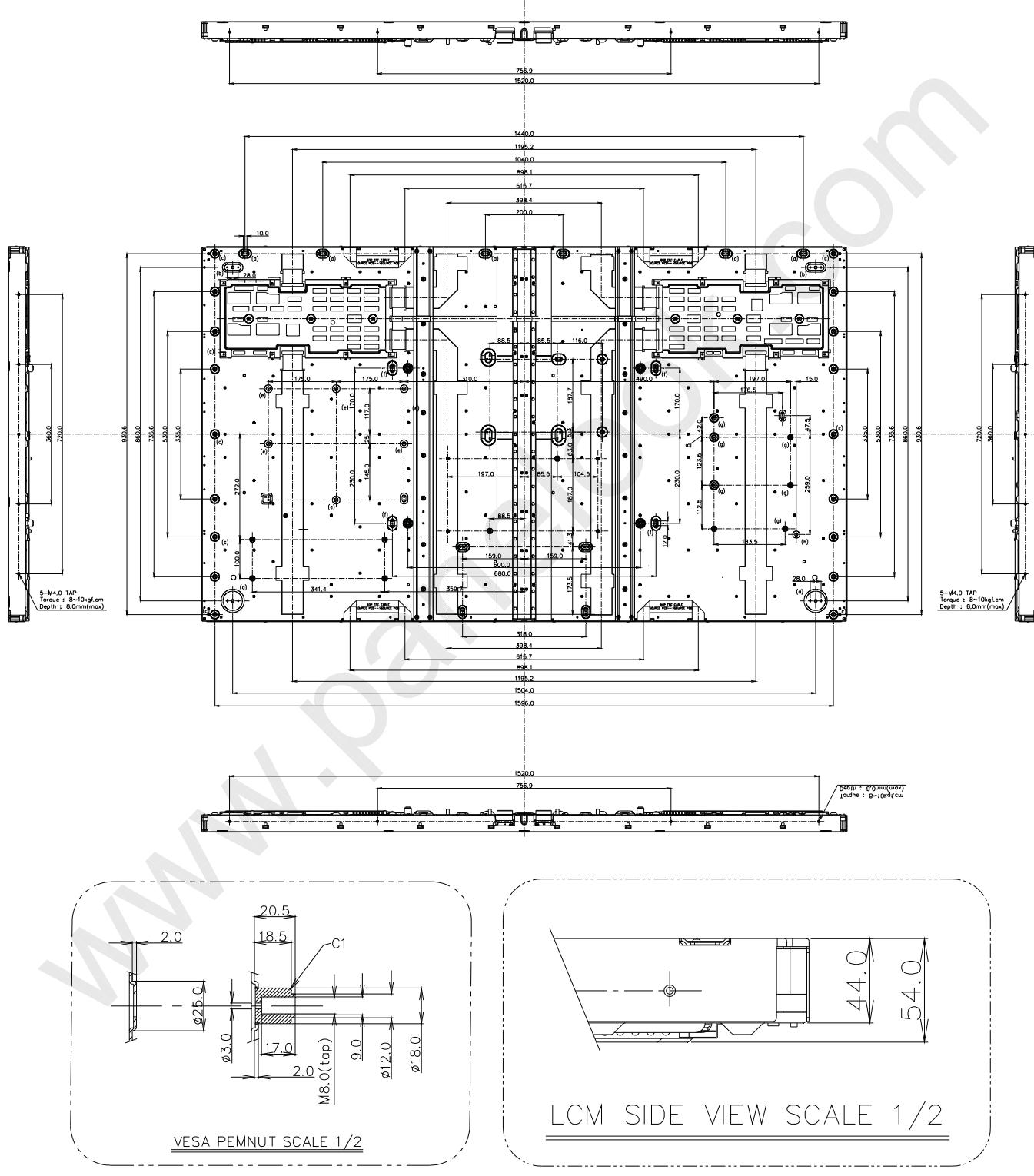
[FRONT VIEW]



LC720DUC

Product Specification

[REAR VIEW]



LC720DUC

Product Specification

6. Reliability

Table 12. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 60°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 50%RH 240h
4	Low temperature operation test	Ta= 0°C 240h
5	Vibration test (non-operating)	Wave form : random Vibration level : 1.0Grms Bandwidth : 10~300Hz Duration : X,Y,Z, 30 min Each direction per 10 min
6	Shock test (non-operating)	Shock level : 10G Waveform : half sine wave, 11ms Direction : ±X, ±Y, ±Z One time each direction
7	Humidity condition Operation	Ta= 40 °C ,90%RH
8	Altitude operating storage / shipment	0 – 15,000 ft 0 – 40,000 ft

Note : Before and after Reliability test, LCM should be operated with normal function.

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Product Specification

7. International Standards

7-1. Safety

- a) UL 60065, Seventh Edition, Underwriters Laboratories Inc.
Audio, Video and Similar Electronic Apparatus - Safety Requirements.
- b) CAN/CSA C22.2 No.60065:03, Canadian Standards Association.
Audio, Video and Similar Electronic Apparatus - Safety Requirements.
- c) EN 60065:2002 + A11:2008, European Committee for Electrotechnical Standardization (CENELEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements.
- d) IEC 60065:2005 + A1:2005, The International Electrotechnical Commission (IEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements.
(Including report of IEC60825-1:2001 clause 8 and clause 9)



TBD

7-2. Environment

- a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

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Product Specification

8. Packing

8-1. Information of LCM Label

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M
---	---	---	---	---	---	---	---	---	---	---	---	---

A,B,C : SIZE(INCH)

E : MONTH

D : YEAR

F ~ M : SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	4	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

- a) Package quantity in one Pallet : 6ea
- b) Pallet Size : 190mm0 X 1140mm X 1248mm

Product Specification

9. Precautions

Please pay attention to the followings when you use this TFT LCD module.

9-1. Mounting Precautions

- (1) You must mount a module using specified mounting holes (Details refer to the drawings).
- (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
- (7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.

9-2. Operating Precautions

- (1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
 $V = \pm 200mV$ (Over and under shoot voltage)
- (2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
- (3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer
- (4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (7) Please do not give any mechanical and/or acoustical impact to LCM. Otherwise, LCM can't be operated its full characteristics perfectly.
- (8) A screw which is fastened up the steels should be a machine screw.
(if not, it can cause conductive particles and deal LCM a fatal blow)
- (9) Please do not set LCD on its edge.
- (10) The conductive material and signal cables are kept away from LED driver inductor to prevent abnormal display, sound noise and temperature rising.

Product Specification

9-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9-5. Storage

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. Handling Precautions for Protection Film

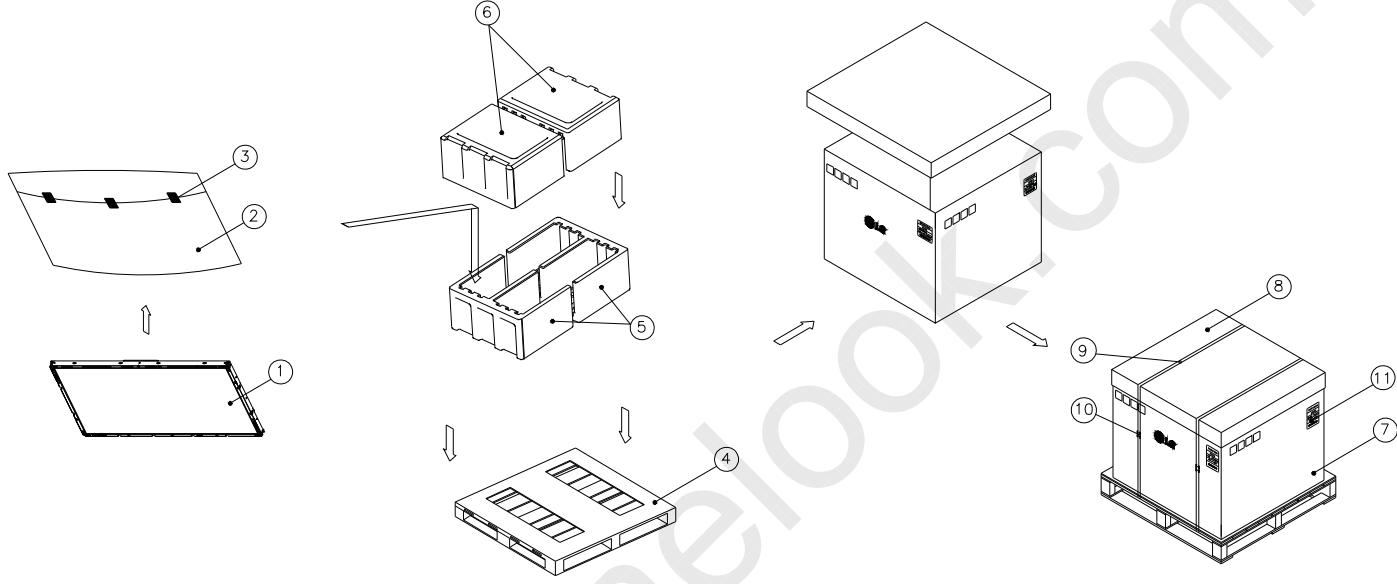
- (1) The protection film is attached to the bezel with a small masking tape.
When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- (2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
- (3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

LC720DUC

Product Specification

APPENDIX-I

■ LC720DUC-SCM1 – Pallet Ass'y



NO.	DESCRIPTION	MATERIAL
1	LCD Module	
2	BAG	72INCH
3	TAPE	MASKING 20MM X 50M
4	PALLET	Plywood (1900X1140X126.5)
5	PACKING	EPS
6	PACKING	EPS
7	ANGLE PACKING	PAPER
8	ANGLE COVER	PAPER
9	BAND,CLIP	STEEL
10	BAND	PP
11	LABEL	YUPO PAPER 80G 100X70

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APPENDIX- II-1

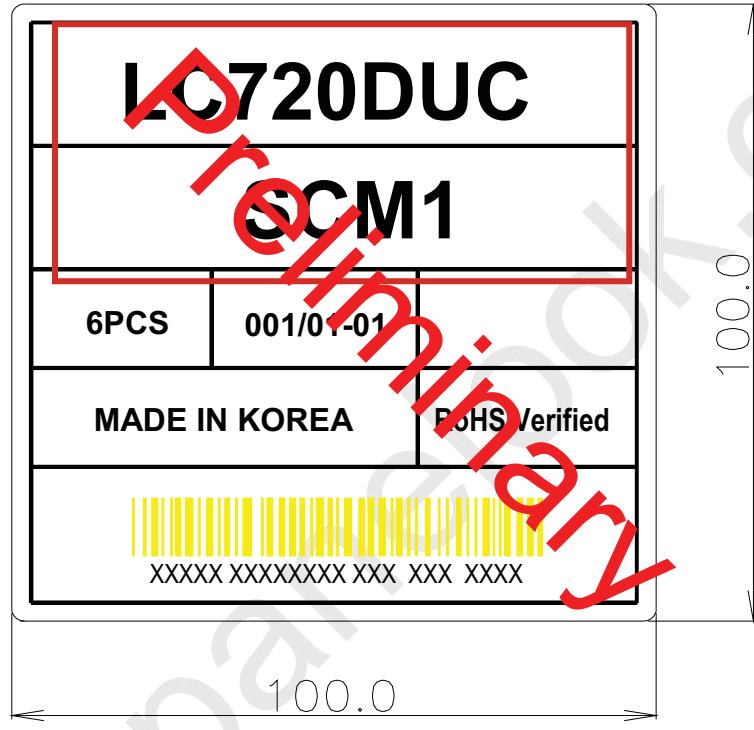
■ LC720DUC-SCM1-LCM Label



LC720DUC

APPENDIX- II-2

■ LC720DUC-SCM1-Pallet Label



LC720DUC

Product Specification

APPENDIX- III-1 Local Dimming Interface Design Guide

► Data Sequence (※ based on 240block)

10-bit : Indicator(1010_0000_00) / Command(10-bit) / Data1(10-bit) / Data2(10-bit) / ... / Data240(10-bit) / check_Sum(10-bit)

10-bit : Indicator(1010_0101) / Command(8-bit) / Data1a(8-bit) / Data1b(8-bit) / ... / Data240b(8-bit) / check_Sum(8-bit)

8-bit : Indicator(1010_1010) / Command(8-bit) / Data1(8-bit) / Data2(8-bit) / ... / Data240(8-bit) / check_Sum(8-bit)

► Data field Definition (※ based on 240block)

1. Indicator Byte : Start of data sequence

2. Command Byte

- Bit 0 : Local-Dimming Enable ('1' : Enable, '0' : Disable)

- Bit 1 : Scanning Enable ('1' : Enable, '0' : Disable)

3D mode 시 ('0': Blinking, '1':Scanning)

- Bit 2 : 3D backlight Enable ('0' : 2D, '1' : 3D)

- Bit 3 : Brightness-up Enable ('1' : Enable, '0' : Disable)

- Bit 4~7 : Reserved (TBD)

3. Data Byte 1 ~ 240 : 8/10-bit Local-dimming gray value

4. Check_Sum Byte = Indicator ^ Command ^ Data1 ^ Data2 ^ ... Data240 (※ ^ : Exclusive OR)

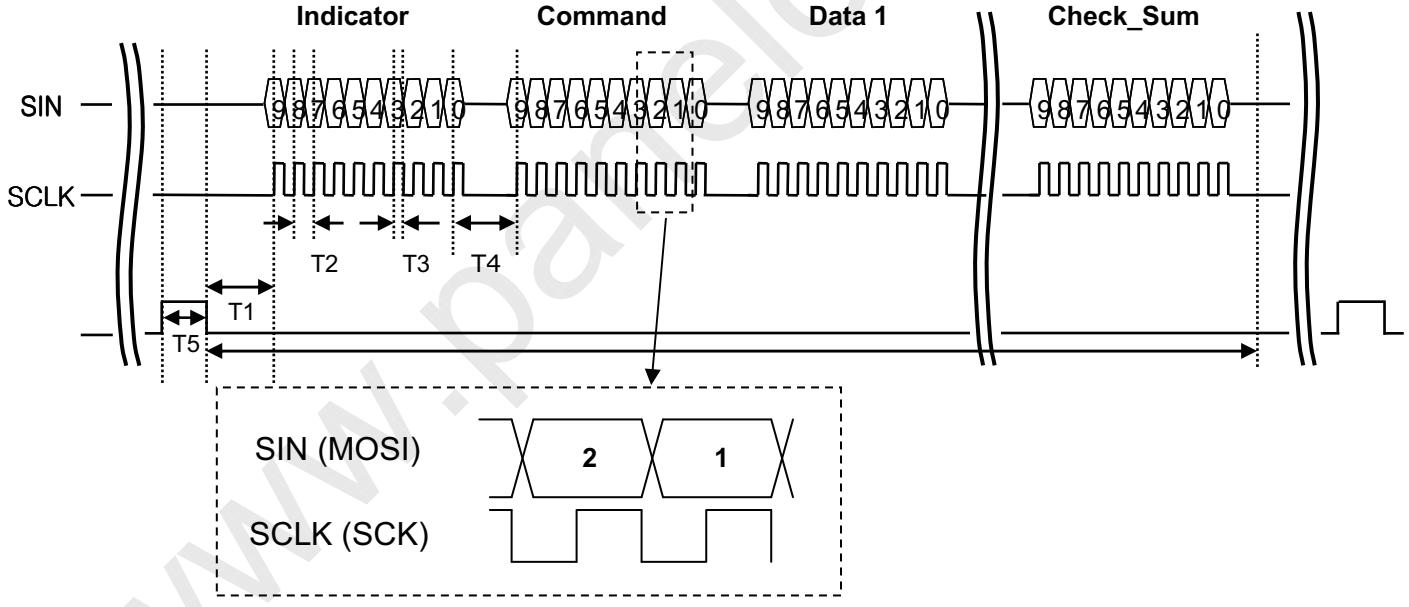


Table15. TIMING TABLE for Local Dimming Interface

* SPI Clock Range : Min 2.5 [MHz], Max 3.0 [MHz]

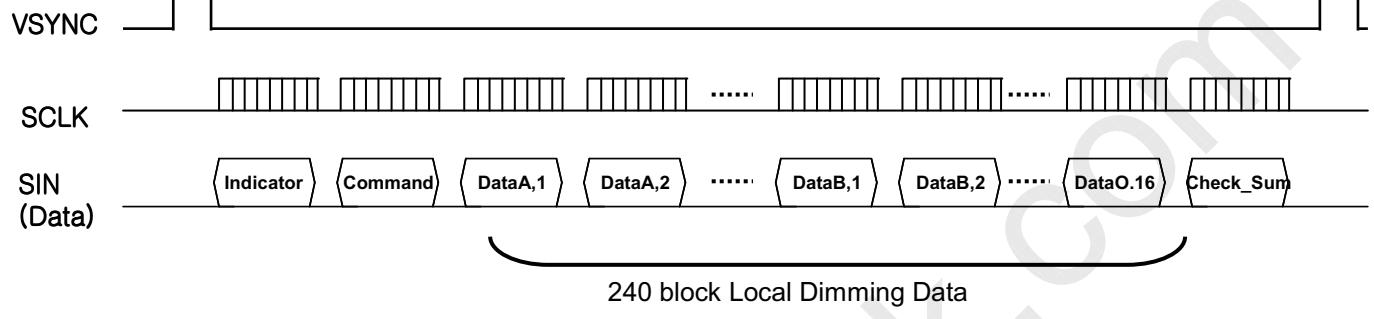
Parameter (DCLK rising edge 기준)	Values			Units
	Min	Typ	Max	
T1	1.000	—	1.200	us
T2	0.333	—	0.400	us
T3	0.167	—	0.200	us
T4	1.000	—	1.200	us
T5	20	—	40	us

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APPENDIX- III-2

■ Local Dimming Block Pin Matching



Front (Left Side, 240Block, 16*15)

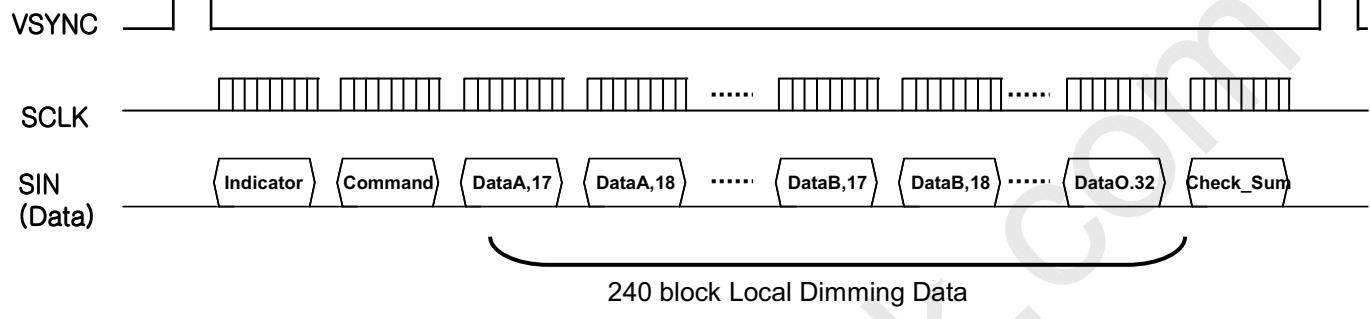
(A,1)	(A,2)	(A,3)	(A,4)	(A,5)	(A,6)	(A,7)	(A,8)	(A,9)	(A,10)	(A,11)	(A,12)	(A,13)	(A,14)	(A,15)	(A,16)
(B,1)	(B,2)	(B,3)	(B,4)	(B,5)	(B,6)	(B,7)	(B,8)	(B,9)	(B,10)	(B,11)	(B,12)	(B,13)	(B,14)	(B,15)	(B,16)
(C,1)	(C,2)	(C,3)	(C,4)	(C,5)	(C,6)	(C,7)	(C,8)	(C,9)	(C,10)	(C,11)	(C,12)	(C,13)	(C,14)	(C,15)	(C,16)
(D,1)	(D,2)	(D,3)	(D,4)	(D,5)	(D,6)	(D,7)	(D,8)	(D,9)	(D,10)	(D,11)	(D,12)	(D,13)	(D,14)	(D,15)	(D,16)
(E,1)	(E,2)	(E,3)	(E,4)	(E,5)	(E,6)	(E,7)	(E,8)	(E,9)	(E,10)	(E,11)	(E,12)	(E,13)	(E,14)	(E,15)	(E,16)
(F,1)	(F,2)	(F,3)	(F,4)	(F,5)	(F,6)	(F,7)	(F,8)	(F,9)	(F,10)	(F,11)	(F,12)	(F,13)	(F,14)	(F,15)	(F,16)
(G,1)	(G,2)	(G,3)	(G,4)	(G,5)	(G,6)	(G,7)	(G,8)	(G,9)	(G,10)	(G,11)	(G,12)	(G,13)	(G,14)	(G,15)	(G,16)
(H,1)	(H,2)	(H,3)	(H,4)	(H,5)	(H,6)	(H,7)	(H,8)	(H,9)	(H,10)	(H,11)	(H,12)	(H,13)	(H,14)	(H,15)	(H,16)
(I,1)	(I,2)	(I,3)	(I,4)	(I,5)	(I,6)	(I,7)	(I,8)	(I,9)	(I,10)	(I,11)	(I,12)	(I,13)	(I,14)	(I,15)	(I,16)
(J,1)	(J,2)	(J,3)	(J,4)	(J,5)	(J,6)	(J,7)	(J,8)	(J,9)	(J,10)	(J,11)	(J,12)	(J,13)	(J,14)	(J,15)	(J,16)
(K,1)	(K,2)	(K,3)	(K,4)	(K,5)	(K,6)	(K,7)	(K,8)	(K,9)	(K,10)	(K,11)	(K,12)	(K,13)	(K,14)	(K,15)	(K,16)
(L,1)	(L,2)	(L,3)	(L,4)	(L,5)	(L,6)	(L,7)	(L,8)	(L,9)	(L,10)	(L,11)	(L,12)	(L,13)	(L,14)	(L,15)	(L,16)
(M,1)	(M,2)	(M,3)	(M,4)	(M,5)	(M,6)	(M,7)	(M,8)	(M,9)	(M,10)	(M,11)	(M,12)	(M,13)	(M,14)	(M,15)	(M,16)
(N,1)	(N,2)	(N,3)	(N,4)	(N,5)	(N,6)	(N,7)	(N,8)	(N,9)	(N,10)	(N,11)	(N,12)	(N,13)	(N,14)	(N,15)	(N,16)
(O,1)	(O,2)	(O,3)	(O,4)	(O,5)	(O,6)	(O,7)	(O,8)	(O,9)	(O,10)	(O,11)	(O,12)	(O,13)	(O,14)	(O,15)	(O,16)

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APPENDIX- III-3

■ Local Dimming Block Pin Matching



Front (Right Side, 240Block, 16*15)

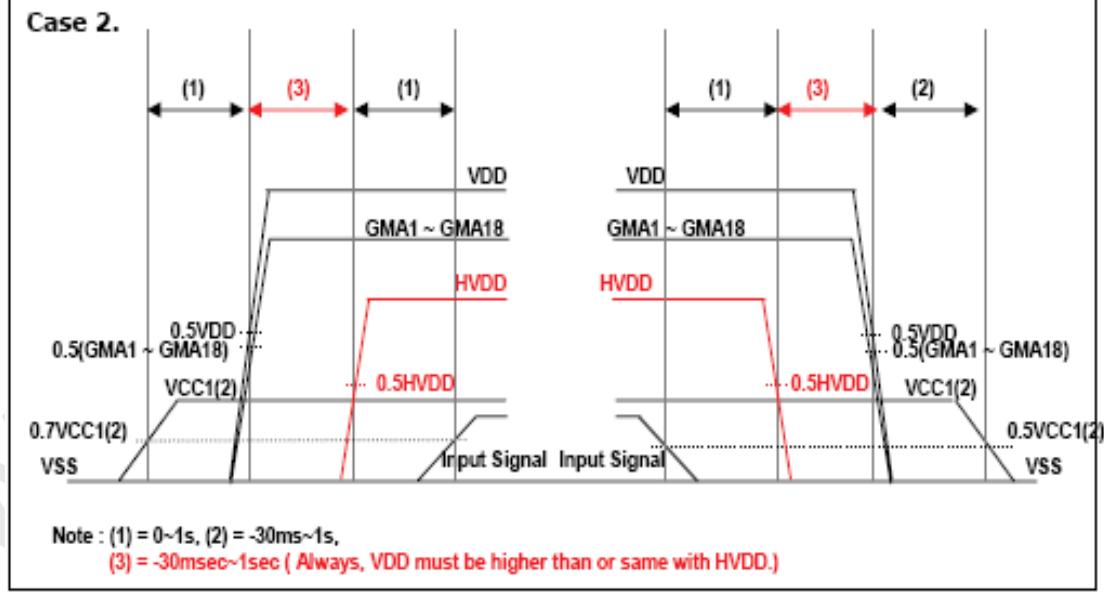
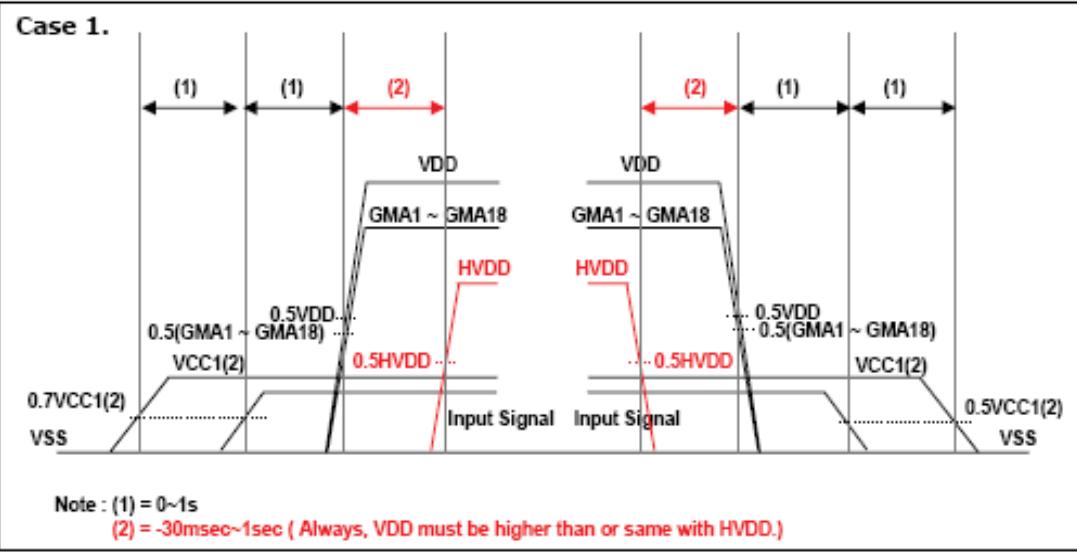
(A,17)	(A,18)	(A,19)	(A,20)	(A,21)	(A,22)	(A,23)	(A,24)	(A,25)	(A,26)	(A,27)	(A,28)	(A,29)	(A,30)	(A,31)	(A,32)
(B,17)	(B,18)	(B,19)	(B,20)	(B,21)	(B,22)	(B,23)	(B,24)	(B,25)	(B,26)	(B,27)	(B,28)	(B,29)	(B,30)	(B,31)	(B,32)
(C,17)	(C,18)	(C,19)	(C,20)	(C,21)	(C,22)	(C,23)	(C,24)	(C,25)	(C,26)	(C,27)	(C,28)	(C,29)	(C,30)	(C,31)	(C,32)
(D,17)	(D,18)	(D,19)	(D,20)	(D,21)	(D,22)	(D,23)	(D,24)	(D,25)	(D,26)	(D,27)	(D,28)	(D,29)	(D,30)	(D,31)	(D,32)
(E,17)	(E,18)	(E,19)	(E,20)	(E,21)	(E,22)	(E,23)	(E,24)	(E,25)	(E,26)	(E,27)	(E,28)	(E,29)	(E,30)	(E,31)	(E,32)
(F,17)	(F,18)	(F,19)	(F,20)	(F,21)	(F,22)	(F,23)	(F,24)	(F,25)	(F,26)	(F,27)	(F,28)	(F,29)	(F,30)	(F,31)	(F,32)
(G,17)	(G,18)	(G,19)	(G,20)	(G,21)	(G,22)	(G,23)	(G,24)	(G,25)	(G,26)	(G,27)	(G,28)	(G,29)	(G,30)	(G,31)	(G,32)
(H,17)	(H,18)	(H,19)	(H,20)	(H,21)	(H,22)	(H,23)	(H,24)	(H,25)	(H,26)	(H,27)	(H,28)	(H,29)	(H,30)	(H,31)	(H,32)
(I,17)	(I,18)	(I,19)	(I,20)	(I,21)	(I,22)	(I,23)	(I,24)	(I,25)	(I,26)	(I,27)	(I,28)	(I,29)	(I,30)	(I,31)	(I,32)
(J,17)	(J,18)	(J,19)	(J,20)	(J,21)	(J,22)	(J,23)	(J,24)	(J,25)	(J,26)	(J,27)	(J,28)	(J,29)	(J,30)	(J,31)	(J,32)
(K,17)	(K,18)	(K,19)	(K,20)	(K,21)	(K,22)	(K,23)	(K,24)	(K,25)	(K,26)	(K,27)	(K,28)	(K,29)	(K,30)	(K,31)	(K,32)
(L,17)	(L,18)	(L,19)	(L,20)	(L,21)	(L,22)	(L,23)	(L,24)	(L,25)	(L,26)	(L,27)	(L,28)	(L,29)	(L,30)	(L,31)	(L,32)
(M,17)	(M,18)	(M,19)	(M,20)	(M,21)	(M,22)	(M,23)	(M,24)	(M,25)	(M,26)	(M,27)	(M,28)	(M,29)	(M,30)	(M,31)	(M,32)
(N,17)	(N,18)	(N,19)	(N,20)	(N,21)	(N,22)	(N,23)	(N,24)	(N,25)	(N,26)	(N,27)	(N,28)	(N,29)	(N,30)	(N,31)	(N,32)
(O,17)	(O,18)	(O,19)	(O,20)	(O,21)	(O,22)	(O,23)	(O,24)	(O,25)	(O,26)	(O,27)	(O,28)	(O,29)	(O,30)	(O,31)	(O,32)

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APPENDIX- IV

■ LC720DUC-SCM1-Source D-IC Power Sequence

**1. Input Signal 정의**

- Input Signal : SOE,POL,GSP,H_CONV,OPT_N